IN THE CLAIMS

1-20. (*Canceled*).

21. (*Currently Amended*) A process for forming an improved trench MOS-gated device, said process comprising:

(a) forming a doped upper layer on a semiconductor substrate, said upper layer having an upper surface and an underlying drain region;

(b) forming a well region having a first polarity in said upper layer, said well region overlying said drain region;

(c) forming a gate trench mask on said upper surface of said upper layer;

(d) forming ~~**a plurality of gate trenches**~~ **at least one gate trench** extending from the upper surface of said upper layer through said well region to said drain region, said gate trenches having sidewalls and floors;

(e) covering said sidewalls and floors with a layer of dielectric material;

(f) filling each of said gate trenches to a selected level substantially below the upper surface of said upper level with a conductive gate material,

(g) removing said trench mask from the upper surface of said upper layer without removing the layer of dielectric material covering said sidewalls of said trenches;

(h) forming an isolation layer of dielectric material on the upper surface of said upper layer and over said dielectric material covering said sidewalls within said gate trench, said isolation layer overlying said gate material and substantially filling said trench;

(i) removing said isolation layer from the upper surface of said upper layer, a portion of said isolation layer remaining within and substantially filling said trench, and having an upper surface that is substantially coplanar with the upper surface of said upper layer,

(j) forming a plurality of heavily doped source regions having a second polarity in said well region, said source regions extending to a selected depth from the upper surface of said upper layer where said selected depth is substantially coplanar with the level of the conductive gate material in the trench, said step of forming **[[a]]** **the** plurality of heavily doped source regions comprising implanting the entire upper surface of said substrate with ions of said second polarity, then forming a body mask on the upper surface of said substrate;

(k) forming a plurality of heavily doped body regions having a first polarity at the upper surface of said upper layer, said body regions overlying the drain region in said upper layer, said step of forming a plurality of heavily doped body regions comprising doping the upper surface of said substrate with a dopant of said first polarity, then removing said body mask; and

(l) forming a metal contact to said body and source regions over the upper surface of said upper layer.

22. (*Original*) The process of claim 21 wherein said substrate comprises monocrystalline silicon.

23. (*Original*) The process of claim 21 wherein said upper layer comprises an epitaxial layer.

24. (*Canceled*).

25. (*Previously Presented*) The process of claim 21 wherein one of said source regions surround said body regions and the source regions are separated from each other by trenches.

26-33. (*Canceled*).

34. (*Previously Presented*) The process of claim 21 wherein said dielectric material covering said sidewalls and said floor, and forming said isolation layer in said gate trench comprises silicon dioxide.

35. (*Original*) The process of claim 21 wherein said conductive gate material within said gate trench is selected from the group consisting of a metal, a silicide, and doped polysilicon.

36. (*Original*) The process of claim 21 wherein the selected level of gate material in the trench is substantially coplanar with the selected depth of the source regions in the upper layer.

37. (*Previously Presented*) The process of claim 21 wherein said first polarization polarity is P and said second polarity is N.

38. (*Canceled*)

39. (*Original*) The process of claim 21 wherein said device is selected from the group consisting of a power MOSFET, an insulated gate bipolar transistor, an MOS-controlled thyristor, and an accumulation FET.

40. (*Currently Amended*) A process for forming an improved trench MOS-gated device, said process comprising:

(a) forming a doped upper layer on a semiconductor substrate, said upper layer having an upper surface and an underlying drain region;

(b) forming a well region having a first polarity in said upper layer, said well region overlying said drain region;

(c) forming a gate trench mask on said upper surface of said upper layer;

(d) forming ~~a plurality of gate trenches~~ **at least one gate trench** extending from the upper surface of said upper layer through said well region to said drain region, said gate trenches having sidewalls and floors;

(e) covering said sidewalls and floors with a layer of dielectric material;

(f) filling each of said gate trenches to a selected level substantially below the upper surface of said upper level with a conductive gate material,

(g) removing said trench mask from the upper surface of said upper layer;

(h) forming an isolation layer of dielectric material on the upper surface of said upper layer and over said dielectric material covering said sidewalls within said gate trench, said isolation layer overlying said gate material and substantially filling said trench;

(i) removing said isolation layer from the upper surface of said upper layer, a portion of said isolation layer remaining within and substantially filling said trench, and having an upper surface that is substantially coplanar with the upper surface of said upper layer,

(j) implanting and diffusing into the surface of the substrate source dopants having a second polarity to form a plurality of heavily doped source regions that extend into the substrate along the sides of the trenches;

(k) implanting and diffusing into the surface a plurality of heavily doped body regions having a first polarity, said body regions overlying the drain region in said upper layer; and

(l) forming a metal contact to said body and source regions over the upper surface of said upper layer.

41. (*Original*) The process of claim 40 wherein the depth of the level of the diffused implants for the source regions is substantially coplanar with the level of the conductive gate material in the trenches.

42. (*New*) A process for forming an improved trench MOS-gated device, said process comprising:

(a) forming a doped upper layer on a semiconductor substrate, said upper layer having an upper surface and an underlying drain region;

(b) forming a well region having a first polarity in said upper layer, said well region overlying said drain region;

(c) forming a gate trench mask on said upper surface of said upper layer;

(d) forming a gate trench extending from the upper surface of said upper layer through said well region to said drain region, said gate trench having sidewalls and a floor;

(e) covering said sidewalls and floor with a layer of gate dielectric material;

(f) filling each of said gate trenches to a selected level with a conductive gate material, said selected level being substantially below the upper surface of said upper level, a portion of said gate dielectric material covering said sidewalls from said selected level to proximate said upper surface of said upper layer;

(g) removing said trench mask from the upper surface of said upper layer without removing said portion of said gate dielectric material covering said sidewalls from said selected level to proximate said upper surface of said upper layer;

(h) forming an isolation layer of dielectric material on the upper surface of said upper layer and over said dielectric material covering said sidewalls within said gate trench, said isolation layer overlying said gate material and substantially filling said trench;

(i) removing said isolation layer from the upper surface of said upper layer, a portion of said isolation layer remaining within and substantially filling

said trench, and having an upper surface that is substantially coplanar with the upper surface of said upper layer,

(j) forming a plurality of heavily doped source regions having a second polarity in said well region, said source regions extending to a selected depth from the upper surface of said upper layer where said selected depth is substantially coplanar with the level of the conductive gate material in the trench, said step of forming a plurality of heavily doped source regions comprising implanting the entire upper surface of said substrate with ions of said second polarity, then forming a body mask on the upper surface of said substrate;

(k) forming a plurality of heavily doped body regions having a first polarity at the upper surface of said upper layer, said body regions overlying the drain region in said upper layer, said step of forming a plurality of heavily doped body regions comprising doping the upper surface of said substrate with a dopant of said first polarity, then removing said body mask; and

(l) forming a metal contact to said body and source regions over the upper surface of said upper layer.